Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN: 1671-5497
E-Publication: Online Open Access
Vol: 42 Issue: 11-2023
DOI: 10.5281/zenodo.10200717

CASCODE FINFET DIRECT COUPLED AMPLIFIER USING CADENCE FINFET TECHNOLOGY

V. SHARMILA
Department of Electronics and Communications Engineering, Vignana Bharathi Institute of Technology, Gathkesar, Telangana Hyderabad. Email: sharmilavallem@gmail.com

CH. KRANTHIREKHA
Department of Electronics and Communications Engineering, Vignana Bharathi Institute of Technology, Gathkesar, Telangana Hyderabad. Email: Kchennaboina20@gmail.com

S. POTHALAIAH
Department of Electronics and Communications Engineering, Vignana Bharathi Institute of Technology, Gathkesar, Telangana Hyderabad. Email: pothalaiahs@gmail.com

SREERAMULA GANGOTHRI
Department of Electronics and Communications Engineering, Vignana Bharathi Institute Technology Gathkesar, Telangana, India. Email: gangothrisreeramula@gmail.com

SUNKARI MANASA
Department of Electronics and Communications Engineering Vignana Bharathi Institute Technology Gathkesar, Telangana, India. Email: mansasunkari2001@gmail.com

KASHIREDDY ANKITHA
Department of Electronics and Communications Engineering, Vignana Bharathi Institute of Technology, Gathkesar, Telangana Hyderabad. Email: ankithareddykashireddy01@gmail.com

Abstract

A direct-coupled amplifier is a type of electronic amplifier where the output of one amplification stage is directly connected to the input of the next stage without the use of coupling capacitors or transformers. This direct connection allows both DC (direct current) and AC (alternating current) signals to pass from one stage to the next. In this paper A cascode amplifier is a two-stage amplifier configuration that combines a common emitter stage directly coupled to a common-base stage, eliminating the need for coupling capacitors. This paper reflects the advantages of using MOSFET Technology for direct coupled common emitter followed by common base amplifier where we try to apply parametric variations in the proposed work which directly reduces the leakage current and hence power consumption in CMOS Technology. In order to improve the circuit performance, we apply parametric variations in the directly coupled common source- common gate MOSFET. In this paper the proposed work shows reduction in leakage current, power consumption, threshold voltage reduction by using parametric variations and FinFET configuration.

Keywords: Power consumption, Cascade amplifier, Parametric Variation, MOSFET, leakage current, power consumption, FinFET.

I. INTRODUCTION

An amplifier is indeed an electronic device or circuit designed to increase the amplitude or strength of an electrical signal [3]. Amplifiers are commonly used in various applications to boost the power of signals, making them suitable for driving speakers, transmitting data over long distances, or processing audio and radio frequency signals. The primary function of an amplifier is to take a weak input signal and produce a stronger output signal

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN: 1671-5497
E-Publication: Online Open Access
Vol: 42 Issue: 11-2023
DOI: 10.5281/zenodo.10200717

with the same shape and characteristics as the input signal, but with a larger amplitude. This amplification process is crucial in many electronic systems to ensure that signals can be transmitted over long distances, heard at sufficient volume, or otherwise processed effectively. Amplifiers play a critical role in electronics and are fundamental components in various electronic devices and systems, allowing for the amplification and processing of signals to meet specific application requirements. The choice of amplifier type and design depends on the specific needs of the application, including factors such as signal frequency, power requirements, distortion tolerance, and cost. An amplifier can be classified based on various criteria including their purpose, operating characteristics, and circuit configurations. An ideal amplifier basically has three main properties: Input resistance, output resistance and gain [5]. A transistor is a semiconductor device that plays a fundamental role in modern electronics as a signal amplifier, switch, or signal modulator. Transistors are essential building blocks in electronic circuits and have revolutionized the field of electronics since their invention. It has three terminals: Emitter, Base and Collector. The common configurations of transistors are based on which terminal is used as the common terminal between input and output. [1].

1) Common-Base (CB) configuration:

The configuration in which the base of the transistor is common between the emitter and collector circuits is indeed called the common base configuration. The transistor in this configuration provides current amplification, and the ratio of the output current (Ic) to the input current (Ie) is known as the current amplification factor, often denoted as "α" (alpha).

The current amplification factor is given in equation (1)

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \qquad (1)$$

The current amplification factor (α) in a common base transistor configuration is typically less than unity, and it approaches unity when the base current reduces to zero. This Configuration provides voltage gain and no current gain.

Common-Emitter (CE) configuration:

The common emitter configuration is one of the three fundamental transistor amplifier configurations, where the emitter terminal is connected between the collector and base.

current amplification factor is given in equation (2)

$$\beta = \frac{\Delta I_C}{\Delta I_B} \qquad (2)$$

The relation between α and β is given in equation (3)

$$\beta = \frac{\alpha}{(1-\alpha)} \qquad (3)$$

The common emitter configuration is commonly used for voltage amplification and provides both voltage gain and current gain. It is widely used in applications such as audio

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN: 1671-5497
E-Publication: Online Open Access
Vol: 42 Issue: 11-2023
DOI: 10.5281/zenodo.10200717

amplifiers, where small input voltage variations result in larger output voltage variations. This configuration offers good power gain and a phase inversion between the input and output signals.

2) Common-Collector (CC) configuration:

The collector is common between the emitter and base, is typically referred to as the "Common Collector" (CC) configuration, also known as the "Emitter Follower" configuration.

current amplification factor is given in equation (4)

$$\gamma = \frac{\Delta I_E}{\Delta I_B} \qquad (4)$$

The relation between α and is given in equation (5)

$$\gamma = \frac{1}{(1-\alpha)} \qquad (5)$$

The Common Collector (CC) configuration provides voltage buffering, high input impedance, and a low output impedance. It is often used in applications where impedance matching is required between a high-impedance source and a low-impedance load. The CC configuration does not provide voltage gain but can provide current gain. the output voltage follows the input voltage with a slight voltage drop, hence the name "Emitter Follower." This configuration is often used in signal buffering and impedance matching applications, particularly when you want to preserve the signal's voltage level while adapting to different impedance levels.

As in whole, we can summarize that CB configuration provides high voltage gain but no current gain, whereas CE configuration provides moderate current and voltage gain. But to be precisely effective, an amplifier should have both high current gain and voltage gain. Thus, to solve this issue we have proposed to use a Cascode CB-CE configuration amplifier.

II. CASCODE AMPLIFER

The cascode technique is a method used to enhance the performance of analog circuits, and it can be applied to both transistors and vacuum tubes, resulting in improved circuit performance. The term "cascode" was first coined in 1939 during a discussion of voltage stabilizer applications by Frederick Vinton Hunt and Roger Wayne Hickman. They proposed a method to replace the pentode vacuum tube by cascoding two triodes to achieve better performance. The cascode amplifier configuration typically comprises two stages: a Common-Emitter (CE) stage and a Common-Base (CB) stage. In this setup, the CE stage feeds into the CB stage. Compared to a single-stage amplifier, this combination offers several distinct characteristics, including high input/output isolation, high input impedance, high output impedance, and a wide bandwidth. In modern circuit design, this amplifier configuration is frequently implemented using two transistors, either Bipolar Junction Transistors (BJTs) or Field-Effect Transistors (FETs). The cascode

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN: 1671-5497
E-Publication: Online Open Access
Vol: 42 Issue: 11-2023
DOI: 10.5281/zenodo.10200717

technique remains an important tool in analog electronics, enabling the creation of high-performance amplifiers and other circuits by taking advantage of the unique characteristics it offers.

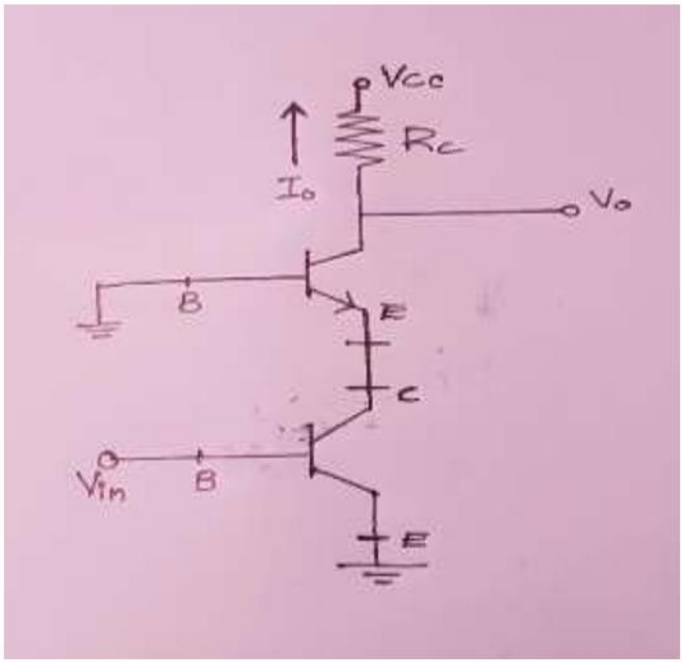

Fig. 1: CE-CB amplifier using BJT

In Fig. 1, we represented a directly coupled CE-CB amplifier using BJT. Here, common emitter (CE) stage followed by a common-base (CB). the circuit results to high current gain & high voltage gain. Along with that, it is also capable of working on high frequencies.

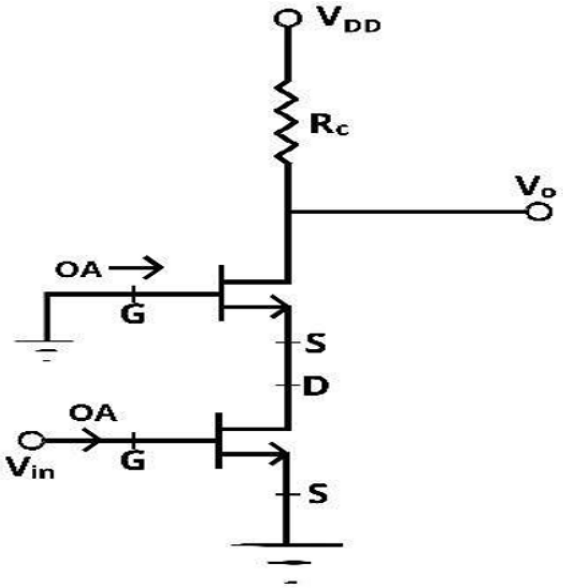

Fig. 2: CG-CS Amplifier using MOSFET

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN: 1671-5497
E-Publication: Online Open Access
Vol: 42 Issue: 11-2023
DOI: 10.5281/zenodo.10200717

This cascode amplifier circuit employs MOSFETs to achieve its amplification function. It consists of two primary stages: an input stage and an output stage. Input Stage: The input stage of this amplifier is built around a common- source MOSFET. The gate terminal of the MOSFET is connected to the input voltage, Vin. As Vin varies, it modulates the current flowing through the common-source MOSFET, resulting in amplification. The amplified signal from the input stage is then passed on to the next stage. Output Stage: The output stage of the cascode amplifier utilizes a common-gate MOSFET configuration. It receives the amplified signal from the common-source MOSFET in the input stage as its input. The common-gate MOSFET in the output stage further amplifies this signal. A drain resistance, Rd, is connected in the output stage, and the output voltage, Vo, can be extracted from the drain terminal of the secondary transistor in this stage. In summary, this cascode amplifier circuit employs MOSFETs to achieve amplification, with the common-source MOSFET in the input stage and the common-gate MOSFET in the output stage. Rd represents the drain resistance, and the output voltage, Vo, can be obtained from the drain terminal of the secondary transistor in the output stage. This configuration offers advantages such as enhanced bandwidth, input/output isolation, and improved amplification, making it suitable for various electronic applications. Further we apply few parametric variations in the following proposed work in order to maximize the current gain.

III. PROPOSED METHOD

In order to improve the circuit performance, we apply parametric variations in the directly coupled common source- common gate MOSFET. By incorporating parametric variations at a particular technology node in MOSFET based amplifier design, we propose to maximize efficiency in terms of power dissipation, and leakage current.

FinFET (Fin-Shaped Field-Effect Transistor)

A FinFET is a specific category of multi-gate Metal- Oxide-Semiconductor Field-Effect Transistor (MOSFET), originally developed at the University of California, Berkeley by Dr. Chenming Hu and his research colleagues. In the context of semiconductor technology, a multi-gate transistor incorporates more than one gate into a single transistor device. The key distinguishing feature of the FinFET is its unique structure, which resembles a set of fins when observed. The structure of a FinFET involves a thin silicon film that is wrapped around and over the conducting channel, forming the transistor's body. This three- dimensional structure allows for improved control over the flow of electrical current. The name "FinFET" is derived from the appearance of these fin-like structures. The crucial aspect to note is that the thickness of the silicon fin, or the semiconductor material used, determines the effective channel length of the device. This channel length is a critical parameter in determining the transistor's performance characteristics. In summary, a FinFET is a type of multi- gate MOSFET with a distinctive 3D structure, where a thin silicon fin forms the body of the transistor. This structure provides enhanced control over the flow of current and has become a fundamental component of advanced semiconductor technology, allowing for smaller, more efficient, and high-performance integrated circuits.

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN: 1671-5497
E-Publication: Online Open Access
Vol: 42 Issue: 11-2023
DOI: 10.5281/zenodo.10200717

The channel length of a MOSFET is defined as the distance between the source and drain junctions. A FinFET is a type of non-planar, double-gate transistor that can be fabricated using either Bulk Silicon-On-Insulator (SOI) or silicon wafers as the substrate material. It is a significant advancement over the traditional single-gate transistor design.

Construction of FinFET

Indeed, the two types of FinFETs, namely Bulk FinFETs and SOI FinFETs, share a common fundamental structure and operate in a manner similar to traditional MOSFETs. The primary distinction lies in the three- dimensional structure known as the "fin" that rises above the silicon substrate.

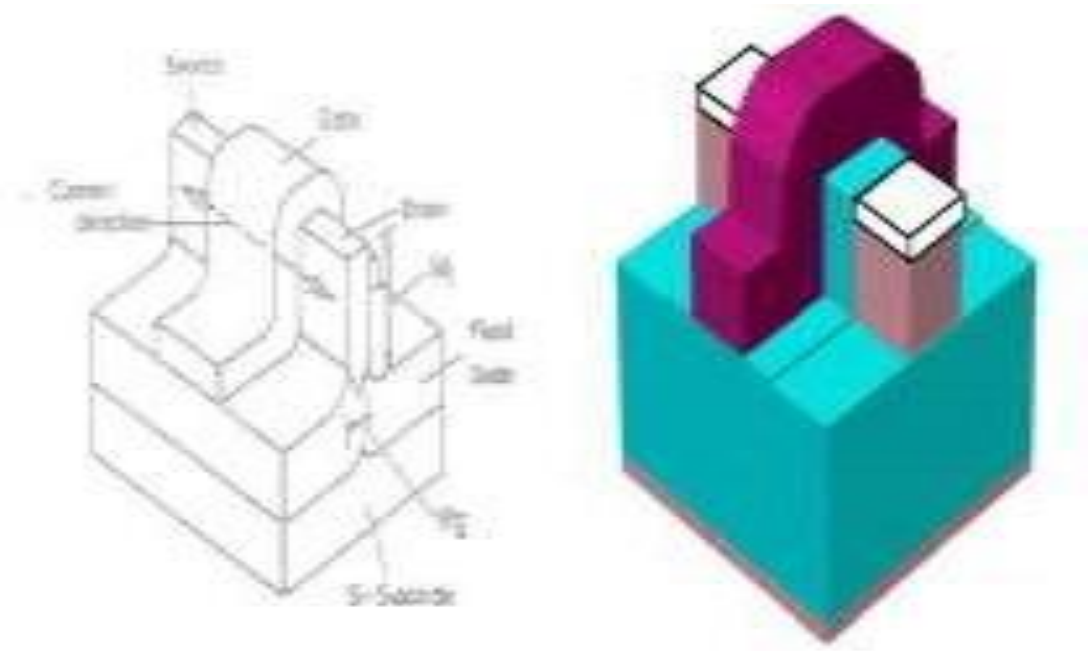

Fig. 3: Construction of Bulk FINFET

Both Bulk FinFETs and SOI FinFETs feature a layout and mode of operation that closely resemble that of conventional MOSFETs. The essential operation involves controlling the flow of electrical current through a semiconductor channel. However, the defining characteristic of FinFETs is the introduction of a three-dimensional structure, known as the "fin," which extends vertically from the silicon substrate. This fin structure is a critical innovation. It allows for more precise control over the channel and offers improved performance in terms of speed, power efficiency, and leakage current control. Despite this structural difference, FinFETs still operate based on the same principles as MOSFETs and are an essential component in modern semiconductor technology, enabling the development of smaller, more efficient, and high- performance integrated circuits. In summary, FinFETs owe their remarkable attributes to their three-dimensional structure, where a thin silicon fin wraps around the conducting channel, leading to enhanced control over the flow of current and superior performance, especially in terms of reducing leakage current and boosting drive current. This innovative design has

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN: 1671-5497
E-Publication: Online Open Access
Vol: 42 Issue: 11-2023
DOI: 10.5281/zenodo.10200717

become a fundamental element in modern semiconductor technology, allowing for the development of smaller, more efficient, and high- performance integrated circuits.

Operation of FinFET

FinFETs are double gated design, the two gates of the FinFET are shorted in the proposed work as shown in Fig

(4) for amplifier design.

This is done to increase the performance and lower the leakages. A Field-Effect Transistor (FET) operates by utilizing an electric field to regulate the conductivity within a channel. The FET's gate terminal has the capability to either allow or inhibit the flow of electrons from the source to the drain, depending on the voltage applied to it.

In this method, the pull-down network comprising of two NMOS in the MOSFET configuration is replaced with two FinFET such that NMOS are placed parallels facing each other with gate, drain, and source terminal shorted with each other. This allows a better control driven gate terminal which was not present in the conventional MOSFET configuration.

The GATE terminal in MOSFET controls the device operation thus as we have shorted the two gate terminals, we are giving more control to the gate in FINFET as compared to MOSFET structure. Another advantage of the FinFET design is that, the proposed work demands lower gate voltage than what was needed to operate the transistor. This leads to better performance of transistor and also reduce power consumption.

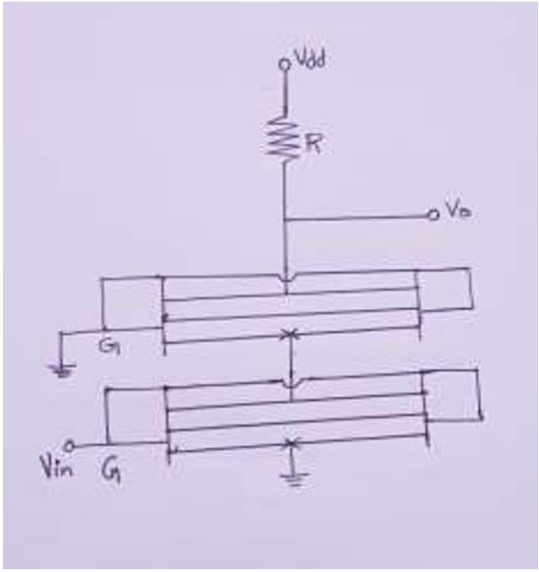

Fig. 4: Proposed FINFET based amplifier design

IV. SCHEMATIC DESIGNS & SIMULATION RESULTS

In this section, we will present the schematic designs and simulation results of the architectural modules discussed in the preceding sections.

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN: 1671-5497
E-Publication: Online Open Access
Vol: 42 Issue: 11-2023
DOI: 10.5281/zenodo.10200717

A. Schematic Design:

The schematics presented here have been designed and implemented using the Cadence Virtuoso platform, utilizing advanced FinFET technology. The implementation of the schematic designs is shown below. Fig. [5] MOSFET base amplifier design schematic. Fig. [6] MOSFET based amplifier design test schematic. Fig. [7] Proposed FinFET based amplifier design schematic. Fig. [8] Proposed FinFET based amplifier design test schematic.

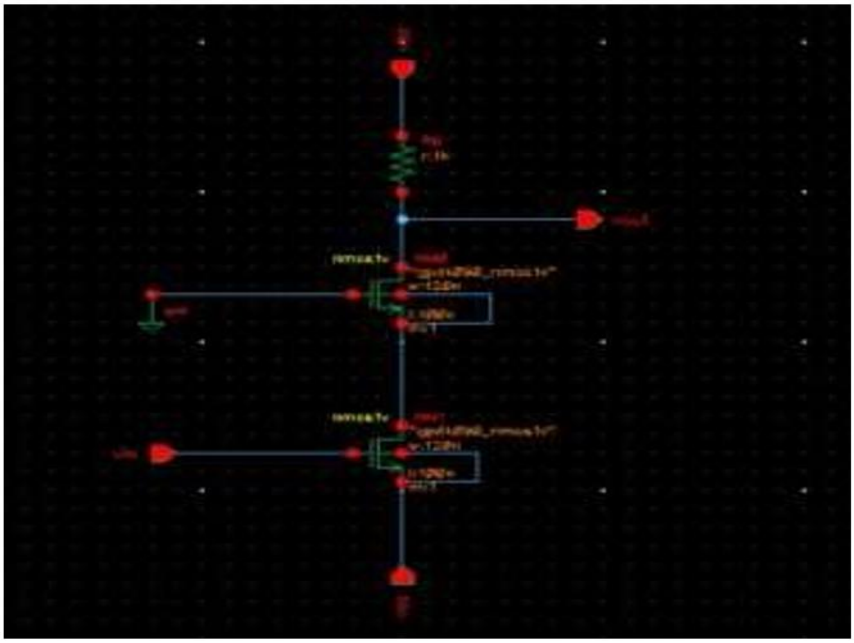

Fig. 5: MOSFET based amplifier design schematic

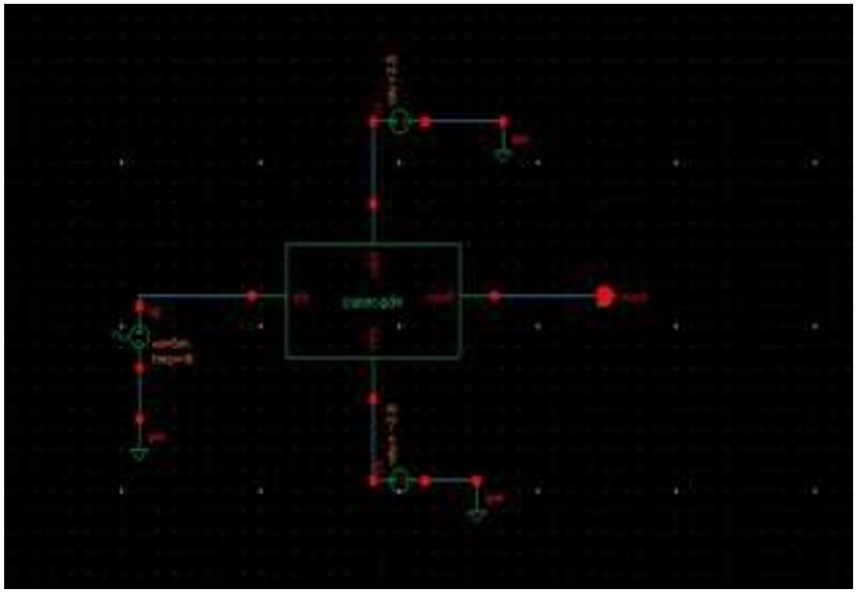

Fig. 6: MOSFET based amplifier design test schematic

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN: 1671-5497
E-Publication: Online Open Access
Vol: 42 Issue: 11-2023
DOI: 10.5281/zenodo.10200717

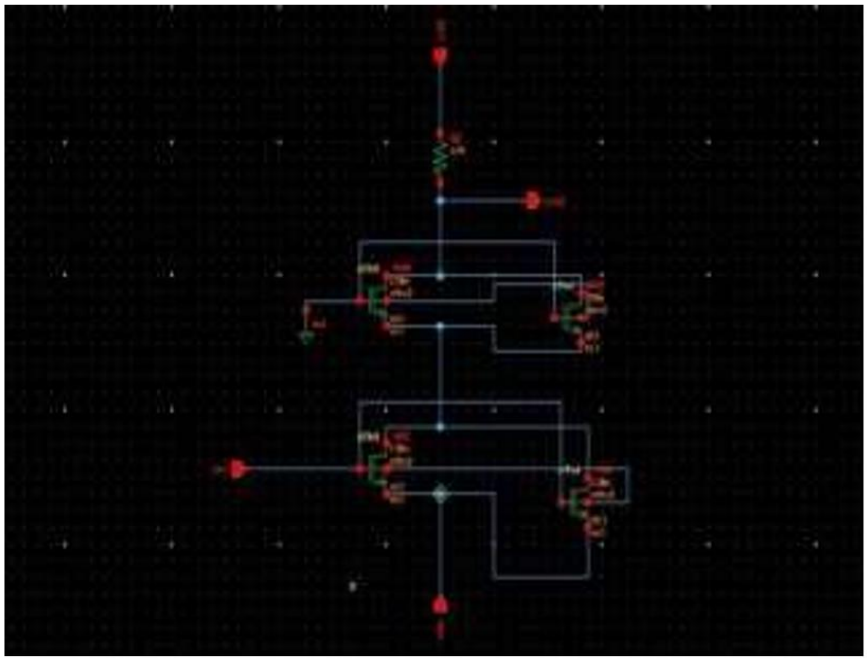

Fig. 7: Proposed FINFET based amplifier design schematic

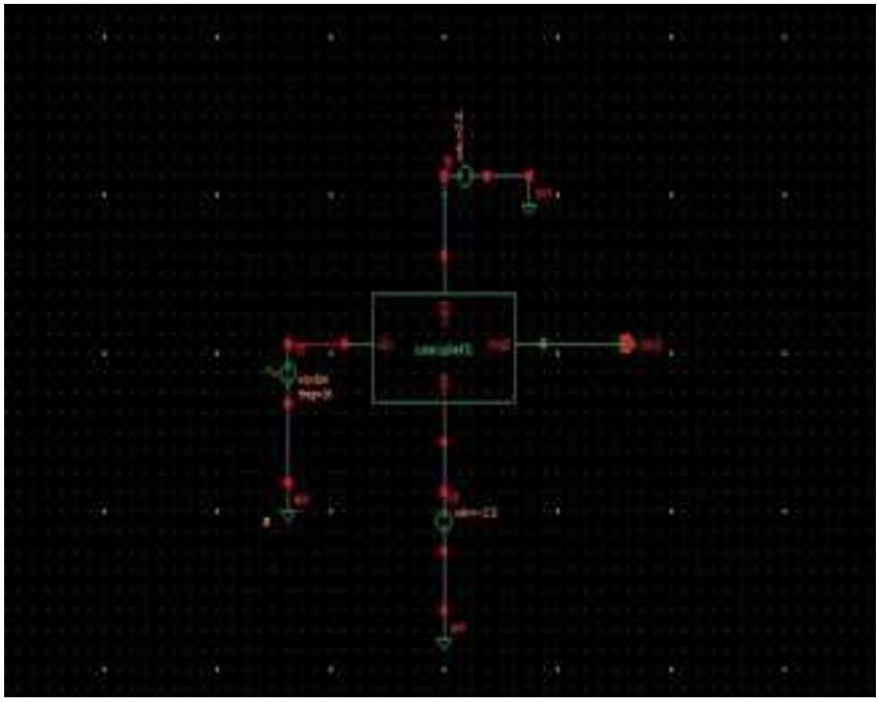

Fig. 8: Proposed FINFET based amplifier design test schematic

Simulation Wave Forms

The schematics have undergone verification and simulation in the Analog Design Environment (ADEL) using the Spectrum Simulation Platform, which employs FinFET

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN: 1671-5497
E-Publication: Online Open Access
Vol: 42 Issue: 11-2023
DOI: 10.5281/zenodo.10200717

technology and operates with a 5mV power supply. Below, Fig. 9 shows Transient Response of MOSFET based amplifier. Fig. 10 shows AC response of MOSFET based amplifier. Fig. 11 shows Transient Response of FINFET based amplifier. Fig. 12 shows AC Response of FINFET based amplifier.

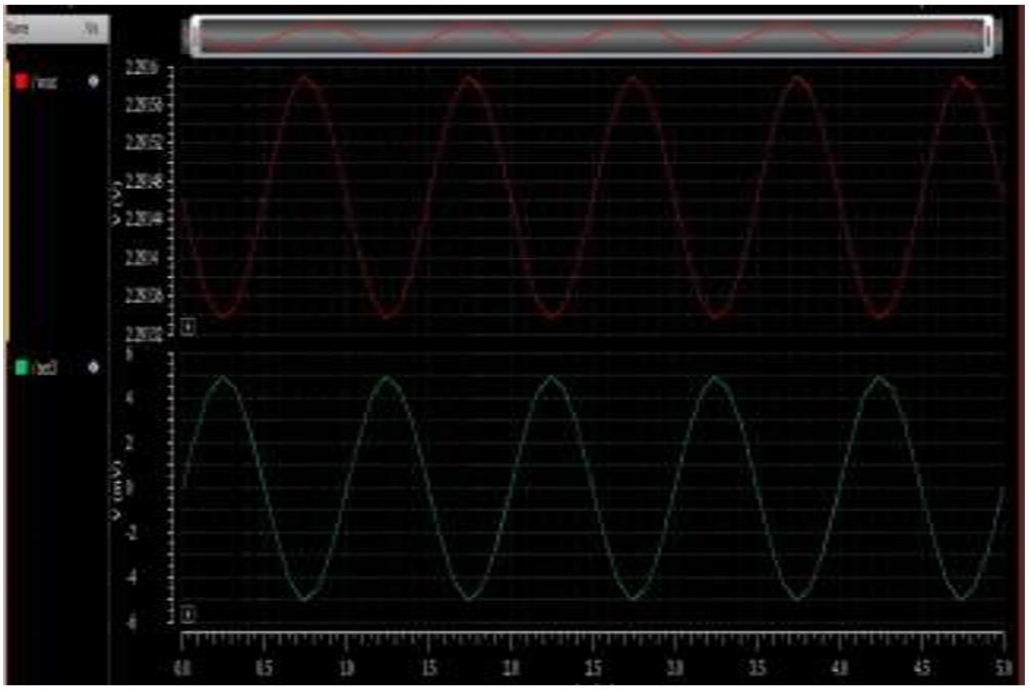

Fig. 9: Transient Response of MOSFET based amplifier

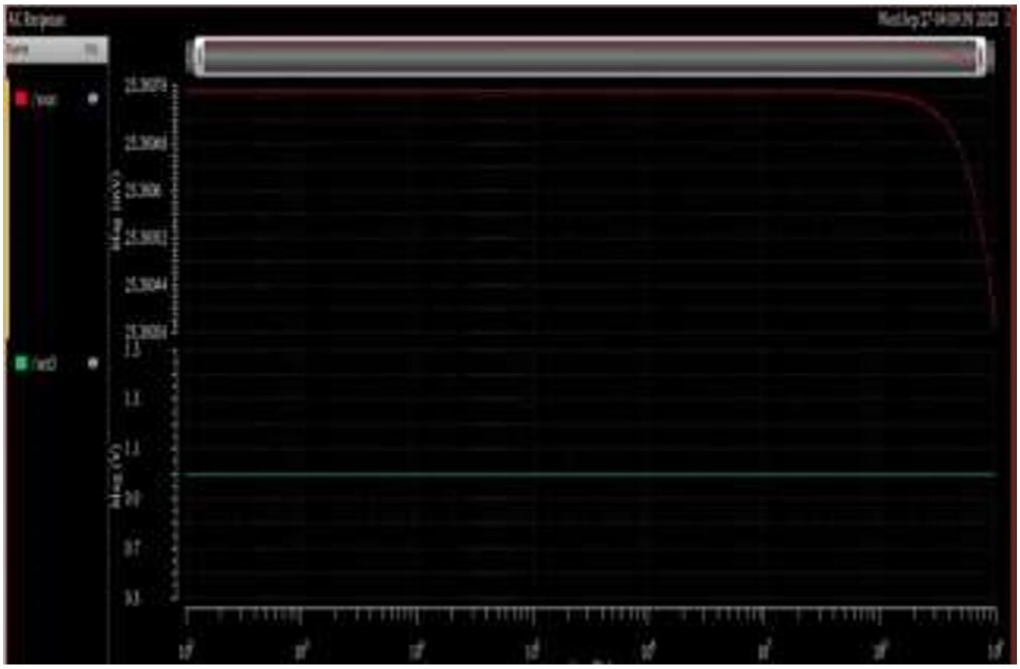

Fig. 10: AC Response of MOSFET based amplifier

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN: 1671-5497
E-Publication: Online Open Access
Vol: 42 Issue: 11-2023
DOI: 10.5281/zenodo.10200717

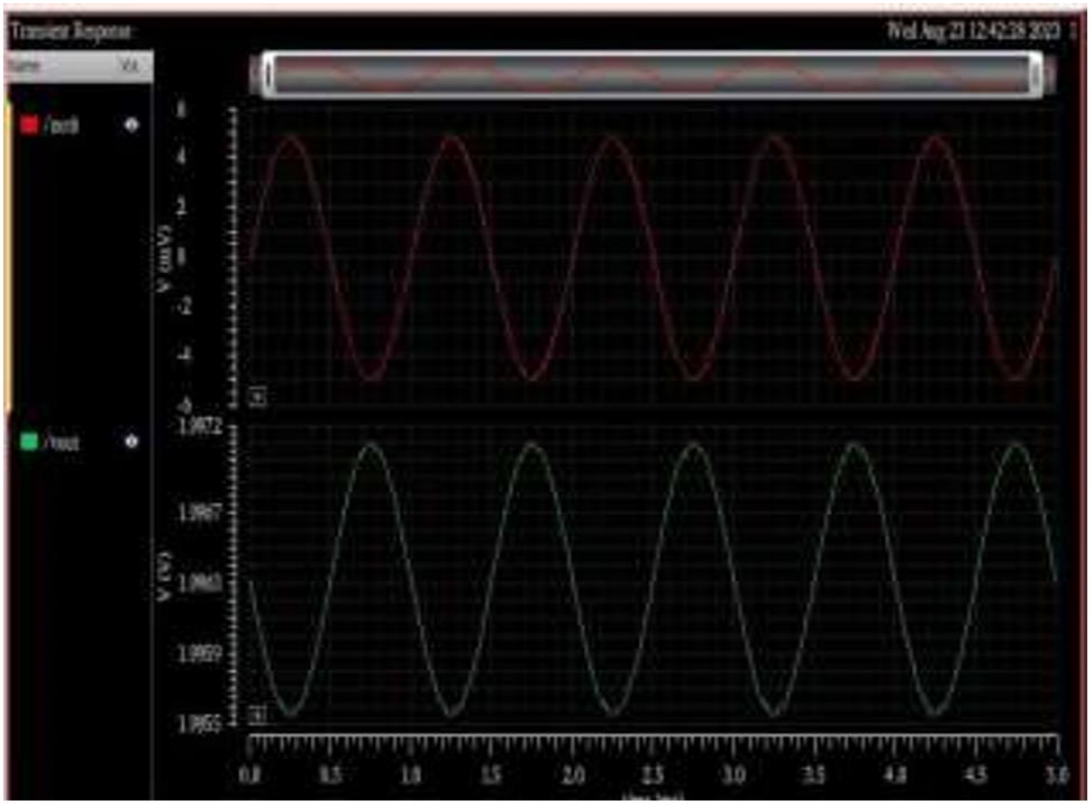

Fig. 11: Transient Response of FINFET based amplifier

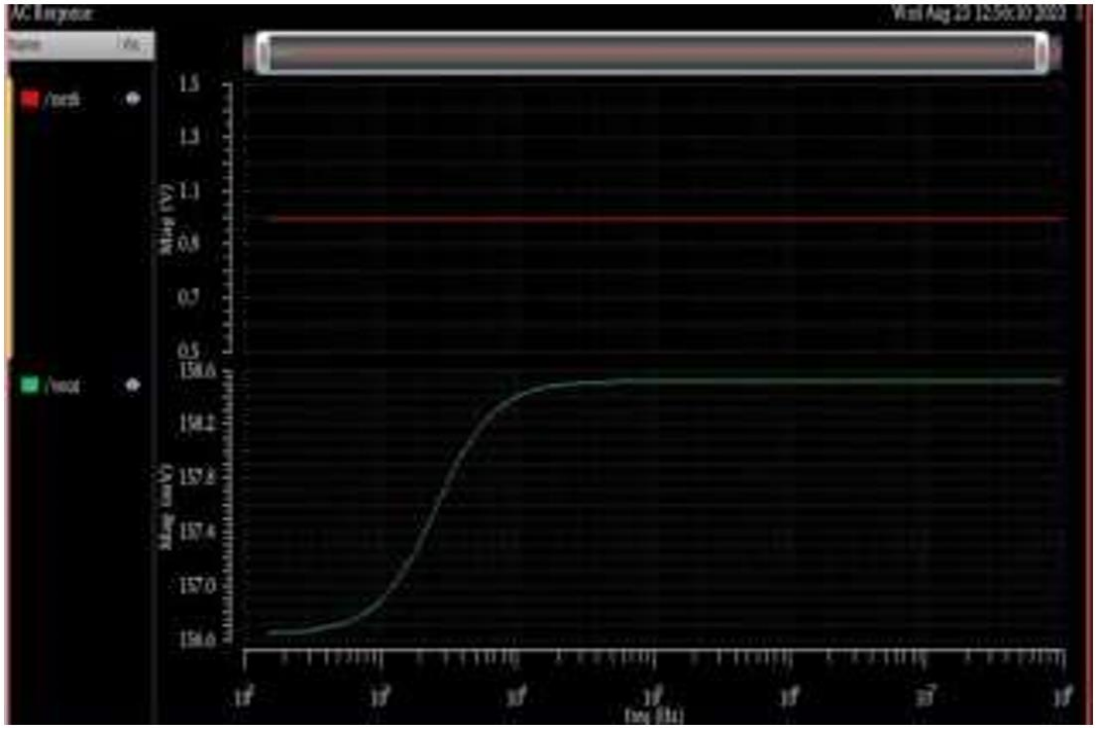

Fig. 12: AC Response of FINFET based amplifier

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN: 1671-5497
E-Publication: Online Open Access
Vol: 42 Issue: 11-2023
DOI: 10.5281/zenodo.10200717

CONCLUSION

FinFETs generate lower leakage power and enable greater device density. FinFET technology's ability to operate at lower voltages, deliver high drive currents, and increase performance density has been pivotal in advancing the semiconductor industry. These features have led to the development of more energy-efficient, powerful, and cost-effective electronic devices across various applications. The proposed work shows reduction in leakage current, power consumption, threshold voltage reduction by using parametric variations and FinFET configuration.

References

1) Shreya Shree, Shweta Bharti, Aditya Pratyush, Pooja Joshi, Chameli Reang, “Cascade FinFET Direct Coupled Amplifier with Power Efficient Technique” IEEE Innovations in energy management and renewable resources 2021.

2) Mohd Haider Hamzah, Asral Bahari Jambek and Uda Hashin, "Design and Analysis of Two -Stage CMOS Op- amp using Silteraa” s 0.13 µ m Technology", *IEEE Symposium on computer application & Industrial Electronics*, April 2014.

3) SachchidaNand Shukla and Susmrita Srivastava “A Novel Circuit Model of Small-Signal Amplifier Developed by Using BJT-JFET- BJT in Triple Darlington Configuration,” International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, vol. 1, Issue 5, November 2012.

4) R. L. Boylestad and L. Nashelsky, Electronic Devices and Circuit Theory, Pearson Education Asia, 3rd ed., Pg.263,307,600, 2002.

5) N. K. Kaphungkui “Two Stage Cascade BJT Amplifier for Very Small Signal Amplification”. International Research Journal of Engineering and Technology, vol. 41, pp 223- 224, 2012.

6) M. N. Ibrahim, H. C. Soh, H. I. Hamzah and A. A. Othman, “Simulation of Single Stage BJT amplifier using LT SPICE”. International research journal of design and communication system, vol 55, pp 27-33, 2016.

7) Praveen Kumar Pandey and Aman Jain, “Design of Low-Voltage Operational Amplifier (700mv),” International Journal of Engineering and Innovative Technology (IJEIT), vol. 3, Issue 1, July 2013.

8) Syan Bandyopadhyay, Deep Mukherjee, Rajdeep Chatterjee, “Design of Two Stage CMOS Operational Amplifier in 180nm technology with Low Power and High CMRR,” ACEEE International Journal of Recent Trends in Engineering & technology, vol. 11, June 2014.

9) Zhang, Q., Zhao, X., Zhang, X. and Zhang, Q., “Multipath recycling method for transconductance enhancement of folded cascade amplifier,” AEU- International Journal of Electronics and Communications, vol. 72, pp.1-7, 2017.

10) Jeong, G., Joo, T. and Hong, S., “ A highly linear and efficient CMOS power amplifier with cascode–cascade configuration,” IEEE Microwave and Wireless Components Letters, vol. 27, pp.596-598, 2017.